be greatly reduced. Further, the semiconductor integrated circuit can be implemented by a chip small in area.

What is claimed is:

1. A method of manufacturing a semiconductor integrated circuit comprised of a plurality of functional blocks respectively provided with predetermined functions by arbitrarily-placed semiconductor devices, comprising the following steps:

a first step for placing a basic cell block comprised of a plurality of basic cells arranged in line and a plurality of functional blocks within a predetermined area of a semiconductor chip;

a second step for designing necessary circuits in the basic cell block; and

a third step for electrically connecting between the basic cells lying within the basic cell block by using interconnections.

2. A method of manufacturing a semiconductor integrated circuit according with claim 1, said basic cell block is laid out by a standard cell system.

3. A method of manufacturing a semiconductor integrated circuit according with claim 1, said first step is laid out by standard cell system or a full custom system.

4. A method of manufacturing a semiconductor integrated circuit according with claim 2, said first step is laid out by standard cell system or a full custom system.

A3

5. A method of manufacturing a semiconductor integrated circuit according with claim 1, said third step is included electrically connecting between said functional blocks by using interconnections.

6. A semiconductor integrated circuit comprising:

a plurality of functional blocks respectively provided with predetermined functions by arbitrarily-placed semiconductor devices;

a basic cell block comprised of a plurality of basic cells arranged in line and electrically connected between the basic cells lying within the basic cell block by using interconnections according to a desired function for implement the desired function.

7. A semiconductor integrated circuit according with claim 6, said functional blocks and said basic cell block is laid out a first area including a center positon in a surface of said semiconductor device.

Subs A3 Cont

8. A semiconductor integrated circuit according with claim 7, said first area surrounded with a second area made up of a plurality of I/O buffers.

9. A semiconductor integrated circuit according with claim 6, a connecting between said basic cells is used by standard cell system.

Add A4

add D9